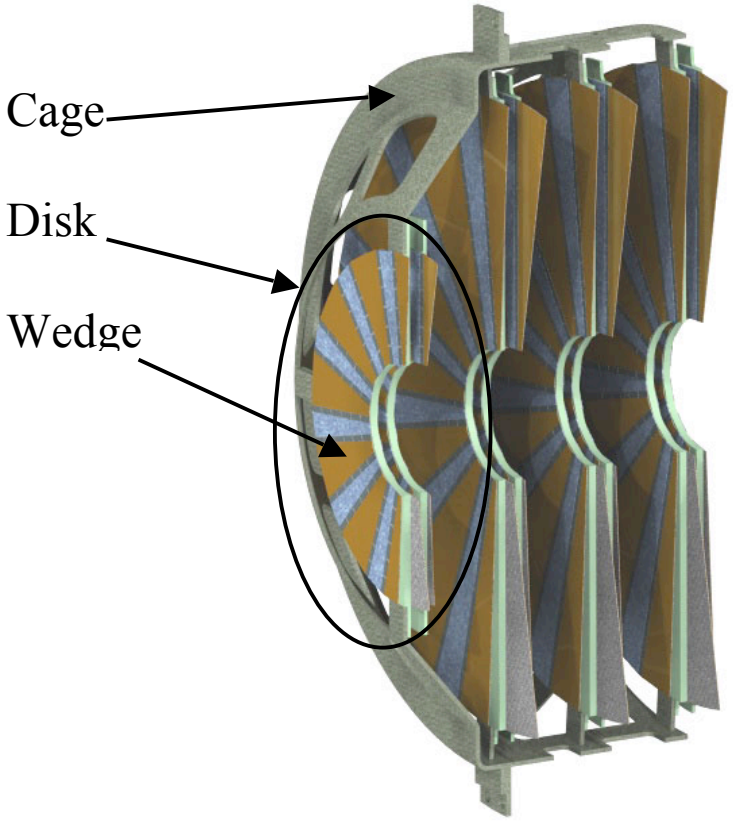
Project Name: PHENIX-FVTX Date: July, 2009
Federal Project Director:
Contract Project Manager: Melynda Brooks, LANL

Reminder of some nomenclature:



Narrative of project highlights:

WBS 1.4.1, Sensor Prototyping: The sensors required for the FVTX project were specified, reviewed internally, and a request for quote for producing sensor prototypes as well as the production sensors was processed through the LANL purchasing department. The contract was awarded to Hamamatsu, and prototype sensors were delivered in October, 2008. Seventeen prototype FVTX sensors were delivered out of 20 requested – the shortfall was due to a manufacturing error. Hamamatsu performed quality acceptance testing on each sensor to ensure that they met our specifications criteria. All specifications were met or exceeded with the following single exception. The maximum resistance value of the polysilicon resistors on the sensors exceeded our maximum specification by about 5%. We accepted this exception because it has no negative impact on sensor performance. Work has been completed at the University of New Mexico to duplicate the Hamamatsu tests. No issues with the Hamamtsu results were found. The process of starting the production procurement started at LANL in May 2009. A new quote was requested and received from Hamamatsu and we expect to place the full order shortly (~July 2009).

WBS 1.4.2, Silicon sensor readout chip (FPHX) prototyping: FNAL completed the design and layout of the FPHX in May 2008 and the chip was submitted to MOSIS June 2, 2008. The prototype chips were received at FNAL on August 21, 2008 where initial power-up and verification of analog output was performed after having a single chip wire-bonded to a test board. The chip was then carried to LANL for more detailed testing of the chip with a test stand which was developed at LANL. All download functionality was exercised, data read-back was performed, and the analog output was studied versus the various chip download parameters. The chip was found to have approximately 200 electrons of noise with no sensor attached, had thresholds which were uniform to within the same noise levels, and the analog output varied with chip download parameters as expected. The noise levels measured (under somewhat less than optimum conditions because several long wire-bonds were included in the setup), can be compared to 115 e + 134 e/pf expected noise levels, based on simulations from the FNAL chip designers. According to the analog engineer, the 200 electrons of measured noise is consistent with the expected baseline noise plus the extra capacitance that is introduced on the front end due to our setup.

Full analog tests, which fully exercised all chip download parameters, were performed by the analog engineer, Tom Zimmerman of FNAL, and he found the chip to perform as expected. Tom has, however, suggested that he can change the physical layout of the chip in such a way as to reduce threshold dispersion among the channels of the chip. We expect to take advantage of this possibility for redesign since he says it is a straight-forward change for the chip.

The digital portion of the chip was further exercised at LANL to check for beam-clock and hit output stability. The chip was pulsed several hundred thousand times with fixed amplitude, fixed spacing between pulses, and fixed numbers of channels unmasked. The data was then checked to see that the ADC output, beam clock number (which should be fixed for these data sets) and channel ID were stable across the entire data set. The relative timing of the pulsing with respect to the beam clock edge was also varied. It was found in these tests that there is an error in the digital chip logic that causes a fraction of beam clock numbers to march out of time when a large number of channels fire at once and when the pulse is near the beam clock edge. The digital designer, Jim Hoff, has since diagnosed the logic problem with the chip and the design fix has been produced and simulated.

We have also tested the chips with up to 26 chips mounted onto an HDI, and bonded or not bonded to a sensor. No new issues have been revealed with our sensor and HDI tests and all chip specifications were met, with the exception of the digital error that was listed above.

A set of all chip modifications required between this round and next round was transferred to FNAL and all of the digital and analog design fixes were implemented. A 2nd round MOSIS submission was placed June 5, 2009. We expect chips from this 2nd round to be delivered in the beginning of August.

WBS 1.4.3, HDI: The kapton HDI layout was completed by UNM and submitted to Dyconex for manufacture. The first prototype HDIs were delivered to UNM March 5, 2009. The bare HDIs were visually inspected and electrically tested to make sure that they matched the schematics, and no issues were uncovered. We then sent a few HDIs to FNAL to have one chip bonded to one HDI and, after the single chip readout was verified to work, we had 13 chips plus a sensor bonded to another HDI. Testing of this original 13-chip assembly was somewhat limited because there were issues applying full sensor bias to the assembly. A new module was assembled and shipped to UNM for testing in June 2009, and to date no issues have been uncovered with testing of this module. Based on this, we believe that we have a full set of revisions that are needed for the next round HDI, and design work for this next round is starting with an Albuquerque designer, working with UNM.

Following our November 2008 FVTX Annual Review, we agreed to in parallel develop a PCB-version HDI so that earlier sensor-readout chip system tests could potentially be performed so that we would be less likely to incur additional schedule delays if the more complex kapton HDI 1st round prototype was not fully functional. The design of this PCB HDI was completed, HDIs were delivered, and tests of up to 13 chips (one full side populated) were completed.

WBS 1.5, DAQ development: The first round ROC prototype board was assembled and delivered to LANL the week of January 11, 2009. The board underwent basic power-up tests by the engineer and was then passed to LANL physicists for more complete tests. We have been exercising the ROC board to read out single chips and the assembled HDI wedges continuously for several months. We uncovered several minor issues with the board, which we were able to patch on the board we have on hand, and the design fixes have already been incorporated into the next rev design. This prototype board is currently being used to read out 4 wedge assemblies, which we plan to insert into a beam at LANL this summer, for final tests of the full wedge assemblies.

This first round prototype ROC board has all the functionality needed for the FVTX detector, but is physically configured to read out prototype detector planes. The layout work for a version needed to read out FVTX planes is in progress at LANL and expected to be completed by the end of August. The first round FEM board layout is also in progress, and is scheduled to be completed by mid-August. A clock distribution board, which will be needed in the Interaction Region, between the counting house and the ROC boards, has been designed, laid out, and procured, but not tested yet. One remaining board, a slow controls interface board which will sit in the FEM VME crates, has been designed and layout is just about complete.

WBS 1.6, Mechanical Design: Final design drawings of the backplane, and cage designs have been completed, pending final review. Some additional work needs to be completed on the final construction drawings for the disks. A PR has been submitted at BNL to procure our production backplanes from LBNL. We have

requested a quote for cage production from LBNL and expect to begin procurement of our production cages once we receive this quote.

WBS 1.4 and 1.7, Assembly Plans: After a visit to the FNAL SiDet laboratory, it was decided to pursue having wedges assembled at SiDet rather than at an FVTX institution(s). SiDet received $15k of construction funds to allow them to work on assembly fixtures and assembly of our first wedge prototypes. To date, SiDet has already assembled or partially assembled 3 kapton HDI modules and 4 PCB HDI modules. SiDet worked with HYTEC and Walter Sondheim to design assembly fixtures, and these were manufactured and used at SiDet with mock-up wedge components, and with the real prototype wedges. A few modifications to fixtures were requested after the prototype wedges were assembled, and updated drawings have been produced. New fixtures will be manufactured once we are confident that no further modifications are needed.

Steve Pate, of NMSU has advanced the disk and full detector assembly plans and started preparing the assembly areas during his sabbatical at BNL from August 2008 – July 2009. Steve worked with Ed O'Brien to identify lab space for assembly, selected two rooms at BNL, and has had them prepared for FVTX occupation. The equipment that is required for assembly and testing tasks was identified and much of this equipment was purchased or acquired from collaborators and installed into the assembly areas.

WBS 1.8, Systems Integration – Walter Sondheim, LANL, has continued to provide the mechanical integration for the project, working with HYTEC on the mechanical design and working with the VTX group to ensure that the VTX and FVTX detectors are compatible with each other inside the enclosure. Eric Mannel has provided the electrical integration for the project, coordinating our electrical reviews, and working with the groups to provide a detailed grounding & shielding plan.

Control milestones covered during review period:

1) **Milestone description:** HDI tested
   Forecast vs actual start/completion date: forecast Q3 FY08, actual Q3 FY09
   Milestone result or impact of delay to project: Electrical tests of the HDIs are completed. The delivered HDIs passed tests of the implementation of the schematics, and clock propagation was tested on a bare HDI and found to be acceptable. After encountering issues biasing the sensor on the first HDI module that was assembled, we went through a process of selecting a new HDI which appeared to have no issues with sensor bias. A sensor and 15 chips were placed on this HDI and tests to date have revealed no issues with the readout. The electrical testing is now complete. One additional test is in process. We wish to perform the bends on the HDI that are needed for production HDIs that will be assembled into the enclosure, and to verify that the HDI continues functioning after bending. A fixture has been designed and is being manufactured by UNM to perform this test.
2) **Milestone Description:** First prototype wedge assembly complete.

Forecast vs actual start/completion date: forecast Q1 FY09, actual Q2 FY09
The first wedge assemblies have been made and tests completed.

3) **Milestone Description:** PHENIX system test complete.
Forecast vs actual start/completion date: forecast Q1 FY09, actual Q2/Q3 FY09
The full system test of up to 26 chips mounted on PCB HDIs and kapton HDIs was completed. No new issues with sensor, readout chip, or HDI design were uncovered in these tests. All design specifications have been met on the components, with the exception of a single design flaw in the FPXH chip, which has been fixed.
4) **Milestone Description:** Review and approve FEM and ROC.
Forecast vs actual start/completion date: forecast Q3 FY09, actual anticipated Q4 FY09
The ROC and FEM design work has been delayed both because funding was diverted away from these tasks in FY09 and because the electrical designer availability within the project is limited enough to not allow them to progress as quickly as projected when we simultaneously had other electrical design projects in progress (PCB HDI design, etc.) The 2nd round ROC and 1st round FEM are still in progress and we are requesting that design work and prototype procurement on both be completed by the end of the summer 2009.
5) **Milestone Description:** Sensor procurement complete.
Forecast vs actual start/completion date: forecast Q3 FY09, actual expected to begin Q3 FY09, completed perhaps in Q4 FY09.
The sensor procurement process was started at LANL in Q3 FY09. A bid has been received from Hamamatsu, all drawings are available, and we expect the actual procurement process to begin shortly.

Brief summary of project issues, concerns, successes:

We were able to complete FPHX tests and redesign work in time for a second round MOSIS submission June 5, 2009. This submission date should allow us to maintain approximately three months of float on our critical path FPHX production if testing of the 2nd round prototype can be completed successfully by approximately the end of August. We are actively working to complete beam tests so that we will have beam tests results by the time we have tested the 2nd round prototype. If we manage to do this, the critical path float should be maintained.

Although the FPHX production has determined our critical path, the other wedge components have been moving closer to the critical path. Backplanes are expected to take longer to produce than initially expected, sensors are being ordered later than we expected, and HDIs are being ordered later than we expected. We are working hard to try to ensure that more components do not move onto the critical path.

Although we have identified electrical designers for HDI redesign, ROC and FEM design, the progress still tends to be a little bit slow because of sharing of resources with other projects. We are working hard to try to ensure that our ROC and FEM prototypes

are completed in time so that we can make our production procurements in January, but continue to have some concerns about whether these schedules will be maintained.

The schedule for backplane production that was received from LBNL is somewhat slower than our project schedule. We are actively working with LBNL to try to ensure that the delivery of backplanes will not hold up production wedge assembly.

The status of cost and schedule is summarized below.

Summary of total expenditures:

A WBS	B ITEM	C Baseline Total Cost (AY$)	D Costed & Committed (AY$)	E Estimate to Complete (AY$)	F Estimated Total Cost (AY$)	G Baseline Contingency (AY$)	H Remaining Contingency (AY$)
1.4.1	Wedge Sensors	1118	126	751	878	206	240
1.4.2	FPHX Chip	692	160	442	602	174	89
1.4.3	HDI	194	50	208	259	39	-64
1.4.4	Flex Cables	70	0	62	62	9	7
1.4 Total		2074	337	1464	1801	428	273
1.5.1	Fiber	21	0	19	19	3	2
1.5.5	Ancillary	246	0	116	116	23	130
1.5.2	ROC	615	68	476	544	139	72
1.5.3	FEM	578	34	401	435	130	143
1.5 Total		1461	101	1012	1114	295	348
1.6.2	Cage	174	77	120	197	35	-23
1.6.3	Wedge Backplane	188	13	134	147	38	41
1.6.4	Support Disk	114	13	73	86	23	28
1.6.5	Jigs	80	15	45	60	15	20
1.6 Total		555	118	372	490	110	65
1.7	Assembly	42	43	-10	33	8	9
1.8	Integration	500	79	308	387	58	113
1.9	Management	249	84	134	218	28	31
Total		790	206	432	638	94	152
Grand Total		**4881**	**762**	**3281**	**4043**	**927**	**838**

The expenditures that have changed since the Management Plan, and how we will cover them are listed here:

- We have shifted part of the FPHX testing funds ($30k) from FNAL to LANL since the FNAL engineers have been only minimally available for testing and Jon Kapustinsky has been instead coordinating these efforts. Since we currently expect only ~$90k of the $145k of funds allocated for FPHX prototype I work at FNAL to be invoiced, we believe this cost is still covered under the FPHX Management Plan costs as listed.
- A total of $30k of sensor testing costs is also being transferred to LANL to cover efforts by Jon Kapustinsky to oversee the testing. This fits within the total sensor testing budget in the Management Plan.

- Following our FVTX Annual Review, we agreed to add a new task to our project: develop and procure a PCB-version HDI to allow sensor and readout chip testing at an earlier date. We estimate this task to cost $40k.
- Clock and DAQ interface boards were not specifically called out in our initial estimate of the DAQ system. As the design evolved, we realized these boards should be separate boards from the ROC/FEM boards. Only a few boards are needed and the design/prototype work is estimated to cost $40k. We do not have enough cost information yet to know if this fits within the ROC/FEM design and production costs as already listed in the Management Plan.
- $37k has been added for ROC FPGA programming and testing of prototype boards.
- We share the costs with the VTX group for Eric Mannel's time for his job of Electrical Integration Manager for the FVTX and VTX projects. We have spent less for WBS 1.8 than was expected in the Management Plan because we budgeted for close to his full salary but paid a smaller fraction because of our cost sharing. For FY08 and FY09 we have spent $61k less than budgeted for this task and will use this savings to cover some of the above added costs.
- We added $30k to the cost to complete the mechanical design work on the cage, backplane and disks, based on updated costs from HYTEC.
- We got a manufacturer's quote on production HDIs. The quote fits within the cost+contingency that we had allocated for the HDIs, but is more than the original cost estimate alone.
- We received an updated quote from LBNL for production of the wedge backplanes. This quote is $147k, compared to our previous estimate of $63k.
- We have received production quotes for FPHX chips and sensors. They are both very comparable to the Management Plan estimates: $410k quote for sensors, compared to $423k in the MP, and the same quote for FPHX chips as was in the MP.
- There is potentially some cost savings in the FPHX prototype chips. The project budgeted for three prototype rounds, but there seems to be a good chance that we will only need two. In addition, the MOSIS runs have been less expensive than what we budgeted and the FNAL testing costs which we have budgeted have been primarily taken care of by FVTX physicists. We have not yet taken into accoun this possible savings.
- We estimate we have $838k remaining contingency, compared to $927k baseline contingency, after all the added costs and savings have been included in the project. The primary contributor to the increased cost, reduced contingency, is the new backplane quote.

Summary of expenditures by FY:

	FY 2008	FY 2009	FY 2010
a) Funds allocated	$500k	$2200.0k	
b) Costs accrued	$144.4 k	$ 581.4k	
c) Uncosted commitments	$264.7 k	$ 224.1k	

d) Uncommitted funds (d=a-b-c)	$90.9	$1403.3k	
e) Remaining total contingency			

Summary of schedule:

	Baseline Start Date mo/year	Baseline Completion Date mo/year	Forecast Start Date mo/year	Forecast Completion mo/year	% Complete Baseline	% Complete Actual
Design						
1.4.1 Sensor*	4/08	7/08	6/08	10/08	100%	95%
1.4.2 FPHX**	10/07	4/08	10/07	5/08	100%	100%
1.5.2 ROC*** 1.5.3 FEM	12/08 12/08	4/09 4/09	12/08 12/08	9/09 8.09	100%	75%
1.4.3 HDI	4/08	8/08	6/08	11/08	100%	95%
1.6.2 Cage****, 1.6.3 wedge, 1.6.4 disk	4/08	10/08	4/08	10/08	100%	95%
Procurement						
1.4.1 Sensor	11/08	6/09	3/09	8/09	100%	25%
1.4.2 FPHX	9/09	12/09	10/09	1/10	0%	0%
1.5.2 ROC 1.5.3 FEM	10/09 10/09	1/10 1/10	1/10 1/10	3/10 3/10	0%	0%
1.4.3 HDI	1/09	3/09	9/09	12/09	100%	0%
Fabrication					0%	0%
1.6.3 Sensor wedge	4/09	11/10	07/09	3/11	10%	0%
1.6.2 Cage, disk	1/09	7/09	6/09	12/09	100%	10%
Operation	3/11	6/11	3/11	6/11	0%	0%

*Sensor Design: design and manufacture prototype
**FPHX Design: 1st round prototype designed
***ROC/FEM Design: start with pre-production prototype, end with prototype produced, tested and approved
****Mechanical Design: final design drawings completed

Summary of control milestones:

WBS Number	Control Milestone Name	Baseline	Actual/

		Date	Forecast Date
WBS 1.1	**DOE construction funds received**	**Q3 FY08**	**Q3 FY08**
Accounts open	**Accounts open**	**Q3 FY08**	**Q3 FY08**
WBS 1.6.2.2.2	**Review and Approve wedge, disk, cage design**	**Q3 FY08**	**Q3 FY08**
WBS 1.4.3.2.5	**HDI tested**	**Q3 FY08**	**Q2 FY09**
WBS 1.4.1.2.3	**Sensor prototype tested**	**Q1 FY09**	**Q1 FY09**
WBS 1.4.1.2.5	**First prototype wedge assembly**	**Q1 FY09**	**Q2 FY09**
WBS 1.5.2.2.6	**PHENIX system test complete**	**Q1 FY09**	**Q3 FY09**
WBS 1.5.2.2.8	**Review and Approve FEM and ROC**	**Q2 FY09**	**Q4 FY09**
WBS 1.4.1.3.1	**Sensor Procurement complete**	**Q3 FY09**	**Q4 FY09**
WBS 1.4.1.2.6	**Wedge assembly test complete**	**Q4 FY09**	**Q4 FY09**
WBS 1.4.2.5.1	**FPHX engineering run complete**	**Q1 FY10**	**Q1 FY10**
WBS 1. 5.3	**ROC and FEM production Complete**	**Q2 FY10**	**Q2 FY10**
WBS 1.7.1.1	**Disk Assembly begins**	**Q3 FY10**	**Q3 FY10**
WBS 1.5.5.6	**Install ancillary Equipment**	**Q4 FY10**	**Q4 FY10**
WBS 1.7.1.1	**Disk Assembly complete**	**Q1 FY11**	**Q1 FY11**
WBS 1.7.2.1 ½	**Cage Assembly finished**	**Q2 FY11**	**Q2 FY11**
WBS 1.7.3	**Install into VTX enclosure**	**Q2 FY11**	**Q2 FY11**
WBS 1.7.3	**Project Complete**	**Q3 FY11**	**Q3 FY11**